Low Power RTC with V_{DD} Battery Backed SRAM and Integrated ±5ppm Temperature Compensation and Auto Day Light Saving

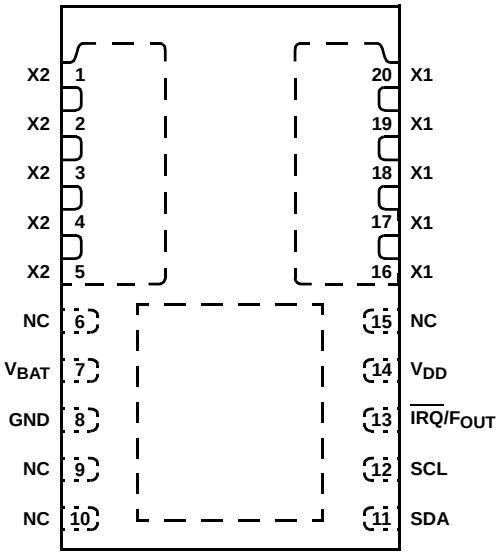
The ISL12020M device is a low power real time clock (RTC) with an embedded temperature sensor for oscillator compensation, clock/calendar, power fail, low battery monitor, brownout indicator, single periodic or polled alarms, intelligent battery backup switching, and 128 bytes of battery-backed user SRAM. The device is offered in a 20 lead DFN module that contains the RTC and an embedded 32.768kHz quartz crystal. The combined device is trimmed to provide less than ±5ppm drift over -40°C to +85°C temperature range.

The RTC tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Daylight Savings time adjustment is done automatically, using parameters entered by the user. Power fail and battery monitors offer user-selectable trip levels. A time stamp function records the time and date of switchover from V_{DD} to V_{BAT} power, and also from V_{BAT} to V_{DD} power.

Pinout

ISL12020M
(20 LD DFN)
TOP VIEW



Features

- Embedded 32.768kHz quartz crystal in the package
- 20 Ld DFN Package
- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes and Seconds
  - Day of the Week, Day, Month and Year
- On-chip Oscillator Temperature Compensation
  - ±5ppm accuracy over -40°C to +85°C
- 10-bit Digital Temperature Sensor Output
  - ±2°C accuracy
- Customer Programmable Day Light Saving Time
- 15 Selectable Frequency Outputs
- 1 Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Super Capacitor
  - Operation to V_{BAT} = 1.8V
  - 1.0µA Battery Supply Current
- Battery Status Monitor
  - 2 User Programmable Levels
  - Seven Selectable Voltages for Each Level
- Power Status Brownout Monitor
  - Six Selectable Trip Levels, from 2.295V to 4.675V
- Oscillator Failure Detection
- Time Stamp for First V_{DD} to V_{BAT}, and Last V_{BAT} to V_{DD} switchover
- 128 Bytes Battery-Backed User SRAM
- I^2C Interface
  - 400kHz Clock Frequency
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- POS Equipment
- Medical Devices
- Printers and Copiers
- Digital Cameras
- Security Systems
- Vending Machine
- White Goods

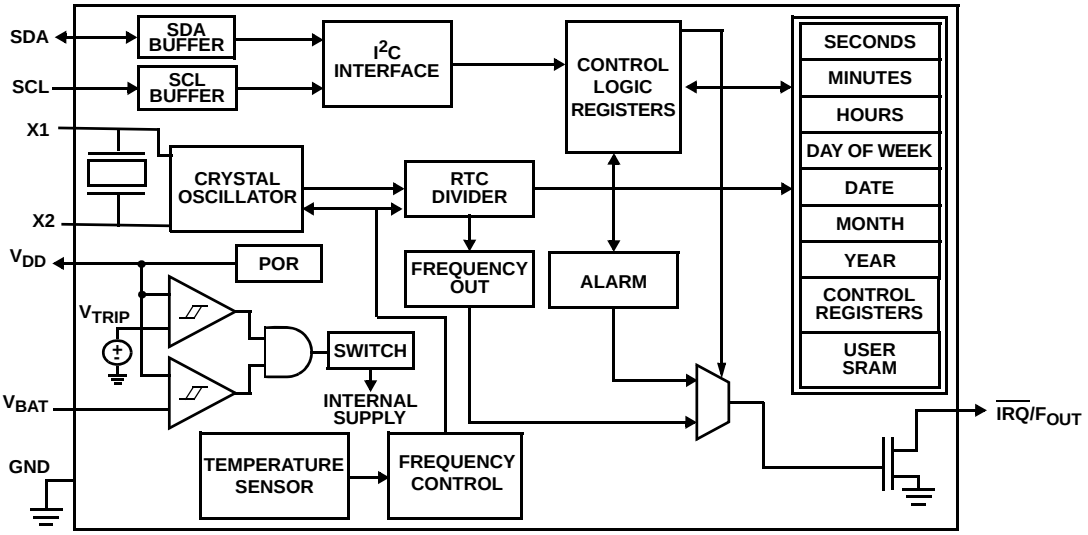
Ordering Information

PART NUMBER (Note)	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG DWG #
ISL12020MIRZ*	ISL12020MIRZ	2.7 to 5.5	-40 to +85	20 Ld DFN	L20.4.0x5.5

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 3, 4, 5	X2	**Crystal Connection.** The X2 pin is the output of an inverting amplifier and is connected to one pin of an integrated 32.768kHz quartz crystal. Do not connect in an application circuit, floating electrical connection.
6, 9, 10, 15	NC	**No connection**. Do not connect to a signal or supply voltage.
7	V_{BAT}	**Backup Supply**. This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
8	GND	**Ground**.
11	SDA	**Serial Data**. SDA is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR’ed with other open drain or open collector outputs.
12	SCL	**Serial Clock**. The SCL input is used to clock all serial data into and out of the device.
13	$\overline{IRQ}/F_{OUT}$	**Interrupt Output/Frequency Output.** Multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the configuration register. The output is open drain and requires a pullup resistor.
14	V_{DD}	**Power supply**.
16, 17, 18, 19, 20	X1	**Crystal Connection**. The X1 pin is the input of an inverting amplifier and is connected to one pin of an internal 32.768kHz quartz crystal. Do not connect in an application circuit, floating electrical connection.

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{IRQ}/F_{OUT}$ pins (respect to ground) . . . . . -0.3V to 6.0V
Voltage on X1 and X2 pins (respect to ground, Note 2) . . . . . -0.3V to 2.5V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3014) . . . . .>3kV
Machine Model . . . . . .>300V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Lead DFN	85	3

Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile (Note 3) . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. The X1 and X2 pins are connected internally to a crystal and should be a floating electrical connection.
3. The ISL12020MOscillator Initial Accuracy can change after solder reflow attachment. The amount of change will depend on the reflow temperature and length of exposure. A general rule is to use only one reflow cycle and keep the temperature and time as short as possible. Changes on the order of ±1ppm to ±3ppm can be expected with typical reflow profiles.

DC Operating Characteristics-RTC Test Conditions: V_{DD} = +2.7 to +5.5V, T_A = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNITS	NOTES
V_{DD}	Main Power Supply		2.7		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	4
I_{DD1}	Supply Current. (I^2C not active, temperature conversion not active, F_{OUT} not active)	V_{DD} = 5V		4.1	6.5	µA	5, 6
		V_{DD} = 3V		3.5	5.5	µA	5, 6
I_{DD2}	Supply Current. (I^2C active, temperature conversion not active, F_{OUT} not active)	V_{DD} = 5V		200	500	µA	5, 6
I_{DD3}	Supply Current. (I^2C not active, temperature conversion active, F_{OUT} not active)	V_{DD} = 5V		120	400	µA	5, 6
I_{BAT}	Battery Supply Current	V_{DD} = 0V, V_{BAT} = 3V, T_A =+25°C		1.0	1.6	µA	5
		V_{DD} = 0V, V_{BAT} = 3V		1.0	5.0	µA	5
I_{BATLKG}	Battery Input Leakage	V_{DD} = 5.5V, V_{BAT} = 1.8V			100	nA	
I_{LI}	Input Leakage Current on SCL	V_{IL} = 0V, V_{IH} = V_{DD}	-1.0	±0.1	1.0	µA	
I_{LO}	I/O Leakage Current on SDA	V_{IL} = 0V, V_{IH} = V_{DD}	-1.0	±0.1	1.0	µA	
V_{BATM}	Battery Level Monitor Threshold		-100		+100	mV	
V_{PBM}	Brownout Level Monitor Threshold		-100		+100	mV	
V_{TRIP}	V_{BAT} Mode Threshold		2.0	2.2	2.4	V	
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			30		mV	9
V_{BATHYS}	V_{BAT} Hysteresis			50		mV	9
$Fout_{25°C}$	Oscillator Initial Accuracy	V_{DD} = 3.3V, T_A = +25°C		±2		ppm	3, 9
$\Delta Fout_T$	Oscillator Stability vs Temperature	V_{DD} = 3.3V	-5		+5	ppm	3, 11
$\Delta Fout_V$	Oscillator Stability vs Voltage	2.7V ≤ V_{DD} ≤ 5.5V	-3		+3	ppm	11
ΔAT_{LSB}	AT Sensitivity per LSB	BETA (4:0) = 10000	0.5	1	2	ppm	11
	Temperature Sensor Accuracy	V_{DD} = V_{BAT} = 3.3V		±2		°C	9
$\overline{IRQ}/F_{OUT}$ (OPEN DRAIN OUTPUT)							
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 3mA			0.4	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			0.4	V	

Power-Down Timing Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNITS	NOTES
V_{DDSR-}	V_{DD} Negative Slew rate				10	V/ms	8

I^2C Interface Specifications Test Conditions: V_{DD}=+2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNITS	NOTES
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05 x V_{DD}			V	9, 10
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} = 5V, I_{OL} = 3mA			0.4	V	
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	9, 10
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	

I^2C Interface Specifications

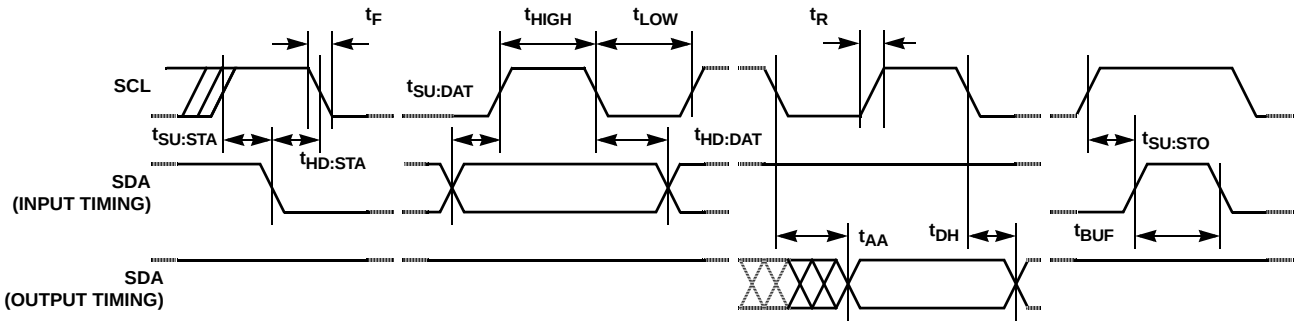
Test Conditions: V_{DD}=+2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 7)	MAX (Note 11)	UNITS	NOTES
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}.			300	ns	10
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}.	20 + 0.1 x Cb		300	ns	10
Cb	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	10
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ	10

NOTES:

4. Temperature Conversion is inactive below V_{BAT} + 1.8V.
5. $\overline{IRQ}/F_{OUT}$ Inactive.
6. $V_{DD} > V_{BAT} + V_{BATHYS}$
7. Specified at +25°C.
8. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
9. Limits should be considered typical and are not production tested.
10. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
11. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

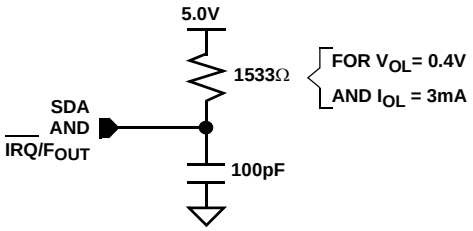


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL12020M device is a low power real time clock (RTC) with embedded temperature sensor and crystal. It contains crystal frequency compensation circuitry over the operating temperature range good to ±5 ppm accuracy. It also contains a clock/calendar with Daylight Savings Time (DST) adjustment, power fail and low battery monitors, brownout indicator, 1 periodic or polled alarm, intelligent battery backup switching and 128 Bytes of battery-backed user SRAM.

The oscillator uses an internal 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction. In addition, both the ISL12020M could be programmed for automatic Daylight Saving Time (DST) adjustment by entering local DST information.

The ISL12020M's alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ}/F_{OUT}$ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or super capacitor with automatic switchover from V_{DD} to V_{BAT}. The ISL12020M device is specified for V_{DD} = 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational in battery backup mode down to 1.8V (Standby Mode). The V_{BAT} level is monitored and reported against preselected levels. The first report is registered when the V_{BAT} level falls below 85% of nominal level, the second level is set for 75%. Battery levels are stored in V_{BATM} registers.

The ISL12020M offers a "Brownout" alarm once the V_{DD} falls below a pre-selected trip level. This allows system Micro to save vital information to memory before complete power loss. There are six V_{DD} levels that could be selected for initiation of the Brownout alarm.

Pin Descriptions

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier and are also connected to the internal 32.768kHz quartz crystal which is the timebase for the real time clock. Compensation circuitry with an internal temperature sensor provides frequency correction to ±5ppm over the operating temperature range from -40°C to +85°C. The X1 and X2 pins are not to be connected to any other circuitry or power voltages, and are best left floating.

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a Super Capacitor or tied to ground if not used. See the Battery Monitor parameter in the "DC Operating Characteristics-RTC" table on page 3.

$\overline{IRQ}/F_{OUT}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the frequency out control bits of the control/status register.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.
- **Frequency Output Mode.** The pin outputs a clock signal, which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain output.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from V_{DD} = 2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12020M for up to 10 years. Another option is to use a super capacitor for applications where V_{DD} is interrupted for up to a month. See the “Application Section” on page 23 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12020M device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 2 and 3.

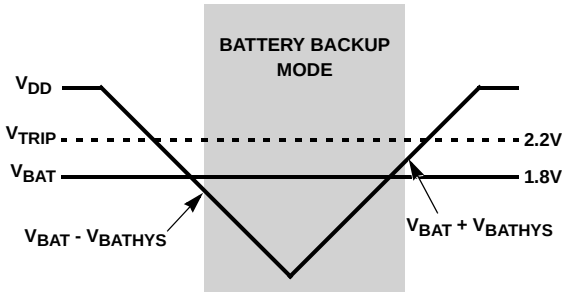


FIGURE 2. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

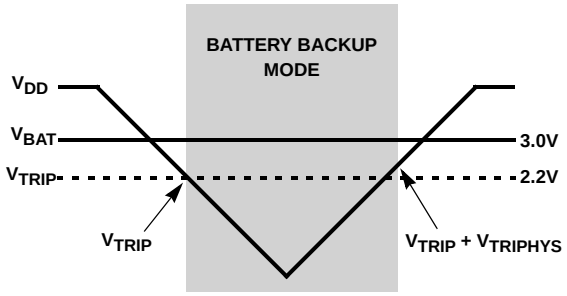


FIGURE 3. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I^2C bus is deactivated in battery backup mode to reduce power consumption. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12020M are active during battery backup mode unless disabled via the control register.

The device Time Stamps the switchover from V_{DD} to V_{BAT} and V_{BAT} to V_{DD}, and the time is stored in t_{SV2B} and t_{SB2V} registers respectively. If multiple V_{DD} power-down sequences occur before status is read, the earliest V_{DD} to V_{BAT} power-down time is stored and the most recent V_{BAT} to V_{DD} time is stored.

Temperature conversion and compensation can be enabled in battery backup mode. Bit BTSE in the BETA register controls this operation, as described in “BETA Register (BETA)” on page 16.

Power Failure Detection

The ISL12020M provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Brownout Detection

The ISL12020M monitors the V_{DD} level continuously and provides warning if the V_{DD} level drops below prescribed levels. There are six (6) levels that can be selected for the trip level. These values are 85% below popular V_{DD} levels. The LVDD bit in the Status Register will be set to “1” when brownout is detected. Note that the I^2C serial bus remains active unless the Battery V_{TRIP} levels are reached.

Battery Level Monitor

The ISL12020M has a built in warning feature once the Back Up battery level drops first to 85% and then to 75% of the battery’s nominal V_{BAT} level. When the battery voltage drops to between 85% and 75%, the LBAT85 bit is set in the status register. When the level drops below 75%, both LBAT85 and LBAT75 bits are set in the status register.

There is a Battery Time Stamp Function available. Once the V_{DD} is low enough to enable switchover to the battery, the RTC time/date are written into the TSVTB register. This information can be read from the TSVTB registers to

discover the point in time of the V_{DD} power-down. If there are multiple power-down cycles before reading these registers, the first values stored in these registers will be retained. These registers will hold the original power-down value until they are cleared by writing “00h” to each register.

The normal power switching of the ISL12020M is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode.

Real Time Clock Operation

The Real Time Clock (RTC) uses an integrated 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12020M powers up after the loss of both V_{DD} and V_{BAT}, the clock will not begin incrementing until at least one byte is written to the clock register.

Single Event and Interrupt

The alarm mode is enabled via the MSB bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low and the alarm status bit (ALM) will be set to “1”.

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to “1”.

The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit). The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, please see “ALARM Registers (10h to 15h)” on page 17.

Frequency Output Mode

The ISL12020M has the option to provide a clock output signal using the $\overline{IRQ}/F_{OUT}$ open drain output pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 1/32Hz to 32kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit.

General Purpose User SRAM

The ISL12020M provides 128 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the I^2C bus is disabled in battery backup mode.

I^2C Serial Interface

The ISL12020M has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL12020M provides both initial timing correction and temperature correction due to variation of the crystal oscillator. Analog and digital trimming control is provided for initial adjustment, and a temperature compensation function is provided to automatically correct for temperature drift of the crystal. Initial values for the initial AT and DT settings (ITR0), temperature coefficient (ALPHA), crystal capacitance (BETA), as well as the crystal turn-over temperature (XTO), are preset internally and recalled to RAM registers on power-up. **These values can be overwritten by the user although this is not suggested as the resulting temperature compensation performance will be compromised.** The compensation function can be enabled/disabled at any time and can be used in battery mode as well.

Register Descriptions

The battery-backed registers are accessible following a slave byte of “1101111x” and reads or writes to addresses [00h:13h]. The defined addresses and default values are described in the Table 1. The battery backed general purpose SRAM has a different slave address (1010111x), so it is not possible to read/write that section of memory while accessing the registers.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 8 sections. They are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (9 bytes): Address 07h to 0Fh.
3. Alarm (6 bytes): Address 10h to 15h.
4. Time Stamp for Battery Status (5 bytes): Address 16h to 1Ah.
5. Time Stamp for V_{DD} Status (5 bytes): Address 1Bh to 1Fh.
6. Day Light Saving Time (8 bytes): 20h to 27h.
7. TEMP (2 bytes): 28h to 29h
8. Crystal Net PPM Correction, NPPM (2 bytes): 2Ah, 2Bh

9. Crystal Turnover Temperature, XT0 (1 byte): 2Ch
10. Crystal ALPHA at high temperature, ALPHA_H (1 byte): 2Dh
11. Scratch Pad (2 bytes): Address 2Eh and 2Fh

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 6 of address 08h) is set to “1”. **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h
07h	CSR	SR	BUSY	OSCF	DSTADJ	ALM	LVDD	LBAT85	LBAT75	RTCF	N/A	01h
08h		INT	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0	N/A	01h
09h		PWR_VDD	CLRTS	D	D	D	D	V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0	N/A	00h
0Ah		PWR_VBAT		RESEALB	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0	N/A	00h
0Bh		ITRO	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	N/A	20h
0Ch		ALPHA	ALPHA7	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0	N/A	46h
0Dh		BETA	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0	N/A	00h
0Eh		FATR	0	0	FFATR5	FATR4	FATR3	FATR2	FATR1	FATR0	N/A	00h
0Fh		FDTR	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0	N/A	00h
10h	ALARM	SCA0	ESCA0	SCA022	SCA021	SCA020	SCA013	SCA012	SCA011	SCA010	00 to 59	00h
11h		MNA0	EMNA0	MNA022	MNA021	MNA020	MNA013	MNA012	MNA011	MNA010	00 to 59	00h
12h		HRA0	EHRA0	D	HRA021	HRA020	HRA013	HRA012	HRA011	HRA010	0 to 23	00h
13h		DTA0	EDTA0	D	DTA021	DTA020	DTA013	DTA012	DTA011	DTA010	01 to 31	00h
14h		MOA0	EMOA00	D	D	MOA020	MOA013	MOA012	MOA011	MOA010	01 to 12	00h
15h		DWA0	EDWA0	D	D	D	D	DWA02	DWA01	DWA00	0 to 6	00h
16h	TSV2B	VSC	0	VSC22	VSC21	VSC20	VSC13	VSC12	VSC11	VSC10	0 to 59	00h
17h		VMN	0	VMN22	VMN21	VMN20	VMN13	VMN12	VMN11	VMN10	0 to 59	00h
18h		VHR	VMIL	0	VHR21	VHR20	VHR13	VHR12	VHR11	VHR10	0 to 23	00h
19h		VDT	0	0	VDT21	VDT20	VDT13	VDT12	VDT11	VDT10	1 to 31	00h
1Ah		VMO	0	0	0	VMO20	VMO13	VMO12	VMO11	VMO10	1 to 12	00h

TABLE 1. REGISTER MEMORY MAP (Continued)

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
1Bh	TSB2V	BSC	0	BSC22	BSC21	BSC20	BSC13	BSC12	BSC11	BSC10	0 to 59	00h
1Ch		BMN	0	BMN22	BMN21	BMN20	BMN13	BMN12	BMN11	BMN10	0 to 59	00h
1Dh		BHR	BMIL	0	BHR21	BHR20	BHR13	BHR12	BHR11	BHR10	0 to 23	00h
1Eh		BDT	0	0	BDT21	BDT20	BDT13	BDT12	BDT11	BDT10	1 to 31	00h
1Fh		BMO	0	0	0	BMO20	BMO13	BMO12	BMO11	BMO10	1 to 12	00h
20h	DSTCR	DstMoFd	DSTE	D	D	DstMoFd20	DstMoFd13	DstMoFd12	DstMoFd11	DstMoFd10	1 to 12	00h
21h		DstDwFd	D	DstDwFdE	DstWkFd12	DstWkFd11	DstWkFd10	DstDwFd12	DstDwFd11	DstDwFd10	0 to 6	00h
22h		DstDtFd	D	D	DstDtFd21	DstDtFd20	DstDtFd13	DstDtFd12	DstDtFd11	DstDtFd10	1 to 31	00h
23h		DstHrFd	D	D	DstHrFd21	DstHrFd20	DstHrFd13	DstHrFd12	DstHrFd11	DstHrFd10	0 to 23	00h
24h		DstMoRv	D	D	D	XDstMoRv20	DstMoRv13	DstMoR12v	DstMoRv11	DstMoRv10	01 to 12	00h
25h		DstDwRv		DstDwRvE	DstWkrv12	DstWkRv11	DstWkRv10	DstDwRv12	DstDwRv11	DstDwRv10	0 to 6	00h
26h		DstDtRv	D	D	DstDtRv21	DstDtRv20	DstDtRv13	DstDtRv12	DstDtRv11	DstDtRv10	01 to 31	00h
27h		DstHrRv	D	D	DstHrRv21	DstHrRv20	DstHrRv13	DstHrRv12	DstHrRv11	DstHrRv10	0 to 23	00h
28h	TEMP	TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00	00 to FF	00h
29h		TK0M	0	0	0	0	0	0	TK09	TK08	00 to 03	00h
2Ah	NPPM	NPPML	NPPM7	NPPM6	NPPM5	NPPM4	NPPM3	NPPM2	NPPM1	NPPM0	00 to FF	00h
2Bh		NPPMH	0	0	0	0	0	NPPM10	NPPM9	NPPM8	00 to 07	00h
2Ch	XT0	XT0	D	D	D	XT4	XT3	XT2	XT1	XT0	00 to FF	00h
2Dh	ALPHA_H	ALPHA_H	ALP_H7	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0	00 to 7F	46h
2Eh	GPM	GPM1	GPM17	GPM16	GPM15	GPM14	GPM13	GPM12	GPM11	GPM10	00 to FF	00h
2Fh		GPM2	GPM27	GPM26	GPM25	GPM24	GPM23	GPM22	GPM21	GPM20	00 to FF	00h

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12020M does not correct for the leap year in the year 2100.

Control and Status Registers (CSR)

Addresses [07h to 0Fh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure (RTCF), Battery Level Monitor (LBAT85, LBAT75), alarm trigger, Daylight Saving Time, crystal oscillator enable and temperature conversion in progress bit.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	BUSY	OSCF	DSTDJ	ALM	LVDD	LBAT85	LBAT75	RTCF

BUSY BIT (BUSY)

Busy Bit indicates temperature sensing is in progress. In this mode, Alpha, Beta and ITRO registers are disabled and cannot be accessed.

OSCILLATOR FAIL BIT (OSCF)

Oscillator Fail Bit indicates that the oscillator has stopped.

DAYLIGHT SAVING TIME CHANGE BIT (DSTADJ)

DSTADJ is the Daylight Saving Time Adjusted Bit. It indicates that the daylight saving time adjustment has happened. DSTADJ is reset to 0 upon power-up. If DST event happens (at either the beginning or the end of DST), DSTADJ will be set to 1. A read of the SR will reset the DSTADJ, or it will be automatically reset on the following month.

ALARM BIT (ALM)

This bit announces if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

LOW V_{DD} INDICATOR BIT (LVDD)

This bit indicates when V_{DD} has dropped below the pre-selected trip level (Brownout Mode). The Trip points for brownout levels are selected by three bits: V_{DD}Trip2, V_{DD}Trip1 and V_{DD}Trip0 in PWR_V_{DD} registers.

LOW BATTERY INDICATOR 85% BIT (LBAT85)

This bit indicates when the battery level has dropped below the pre-selected trip levels (85% of battery voltage). The trip points are selected by three bits: VB85Tp2, VB85Tp1 and VB85Tp0 in the PWR_VBAT registers.

LOW BATTERY INDICATOR 75% BIT (LBAT75)

This bit indicates when the battery level has dropped below the pre-selected trip levels (75% of battery voltage). The trip points are selected by three bits: VB75Tp2, VB75Tp1 and VB75Tp0 in the PWR_VBAT registers.

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12020M internally) when the device powers up after having lost all power (defined as V_{DD} = 0V and V_{BAT} = 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

Interrupt Control Register (INT)

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0

AUTOMATIC RESET BIT (ARST)

This bit enables/disables the automatic reset of the ALM, LVDD, LBAT85, and LBAT75 status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the ALM, LVDD, LBAT85, and LBAT75 bits.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}/F_{OUT}$ pin when the RTC is triggered by the alarm, as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ}/F_{OUT}$ pin will be set low until the ALM status bit is cleared to “0”.

TABLE 4.

IM BIT	INTERRUPT/ALARM FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the $\overline{IRQ}/F_{OUT}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to “1”, the $\overline{IRQ}/F_{OUT}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to “0”, the $\overline{IRQ}/F_{OUT}$ pin is enabled during battery backup mode. Note that the open drain $\overline{IRQ}/F_{OUT}$ pin will need a pull-up to the battery voltage to operate in battery backup mode.

FREQUENCY OUT CONTROL BITS (FO<3:0>)

These bits enable/disable the frequency output function and select the output frequency at the $\overline{IRQ}/F_{OUT}$ pin. See Table 5 for frequency selection. Default for the ISL12020M is FO<3:0> = 1h, or 32.768kHz output (F_{OUT} is **ON**). When the frequency mode is enabled, it will override the alarm mode at the $\overline{IRQ}/F_{OUT}$ pin.

TABLE 5. FREQUENCY SELECTION OF $\overline{IRQ}/F_{OUT}$ PIN

FREQUENCY, F_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

POWER SUPPLY CONTROL REGISTER (PWR_VDD)

Clear Time Stamp Bit (CLRTS)

ADDR	7	6	5	4	3	2	1	0
09h	CLRTS	0	0	0	0	V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0

This bit clears Time Stamp V_{DD} to Battery (TSV2B) and Time Stamp Battery to V_{DD} Registers (TSB2V). The default setting is 0 (CLRTS = 0) and the Enabled setting is 1 (CLRTS = 1).

V_{DD} Brownout Trip Voltage BITS (V_{DD}Trip<2:0>)

These bits set the trip level for the V_{DD} alarm, indicating that V_{DD} has dropped below a preset level. In this event, the LVDD bit in the Status Register is set to “1”. See Table 6.

TABLE 6. V_{DD} TRIP LEVELS

V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0	TRIP VOLTAGE (V)
0	0	0	2.295
0	0	1	2.550
0	1	0	2.805
0	1	1	3.060
1	0	0	4.250
1	0	1	4.675

Battery Voltage Trip Voltage Register (PWR_VBAT)

This register controls the trip points for the two V_{BAT} alarms, with levels set to approximately 85% and 75% of the nominal battery level.

TABLE 7.

ADDR	7	6	5	4	3	2	1	0
0Ah	D	RESEALB	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0

RESEAL BIT (RESEALB)

This is the Reseal bit for actively disconnecting V_{BAT} pin from the internal circuitry. Setting this bit allows the device to disconnect the battery and eliminate standby current drain while the device is unused. Once V_{DD} is powered up, this bit is reset and the V_{BAT} pin is then connected to the internal circuitry.

The application for this bit involves placing the chip on a board with a battery and testing the board. Once the board is tested and ready to ship, it is desirable to disconnect the battery to keep it fresh until the board or unit is placed into final use. Setting RESEALB = “1” initiates the battery disconnect, and after V_{DD} power is cycled down and up again, the RESEAL bit is cleared to “0”.

BATTERY LEVEL MONITOR TRIP BITS (VB85TP<2:0>)

Three bits select the first alarm (85% of Nominal V_{BAT}) level for the battery voltage monitor. There are total of 7 levels that could be selected for the first alarm. Any of the of levels could be selected as the first alarm with no reference as to nominal Battery voltage level. See Table 8.

TABLE 8. VB85T ALARM LEVEL

VB85Tp2	VB85Tp1	VB85Tp0	BATTERY ALARM TRIP LEVEL (V)
0	0	0	2.125
0	0	1	2.295
0	1	0	2.550
0	1	1	2.805
1	0	0	3.060
1	0	1	4.250
1	1	0	4.675

BATTERY LEVEL MONITOR TRIP BITS (VB75TP<2:0>)

Three bits select the second alarm (75% of Nominal V_{BAT}) level for the battery voltage monitor. There are total of 7 levels that could be selected for the second alarm. Any of the of levels could be selected as the second alarm with no reference as to nominal Battery voltage level. See Table 9.

TABLE 9. BATTERY LEVEL MONITOR TRIP BITS (VB75TP<2:0>)

VB75Tp2	VB75Tp1	VB75Tp0	BATTERY ALARM TRIP LEVEL (V)
0	0	0	1.875
0	0	1	2.025
0	1	0	2.250
0	1	1	2.475
1	0	0	2.700
1	0	1	3.750
1	1	0	4.125

Initial AT and DT setting Register (ITRO)

These bits are used to trim the initial error (at room temperature) of the crystal. Both Digital Trimming (DT) and Analog Trimming (AT) methods are available. The digital trimming uses clock pulse skipping and insertion for frequency adjustment. Analog trimming uses load capacitance adjustment to pull the oscillator frequency. A range of +62.6ppm to -61.5ppm is possible with combined digital and analog trimming.

Initial values for the ITR0 register are preset internally and recalled to RAM registers on power-up. **These values can be overwritten by the user although this is not suggested as the resulting temperature compensation performance will be compromised.** Aging adjustment is normally a few ppm and can be handled by writing to the IATR section.

AGING AND INITIAL TRIM DIGITAL TRIMMING BITS (IDTR0<1:0>)

These bits allow ±30.5ppm initial trimming range for the crystal frequency. This is meant to be a coarse adjustment if the range needed is outside that of the IATR control. See Table 10. The IDTR0 register should only be changed while the TSE (Temp Sense Enable) bit is “0”.

The ISL12020M has a preset Initial Digital Trimming value corresponding to the crystal in the module. This value is recalled on initial power-up and should never be changed for best temperature compensation performance, although the user may change this preset value to adjust for aging or board mounting changes if so desired.

TABLE 10. IDTR0 TRIMMING RANGE

IDTR01	IDTR00	TRIMMING RANGE
0	0	Default/Disabled
0	1	+30.5ppm
1	0	0ppm
1	1	-30.5ppm

AGING AND INITIAL ANALOG TRIMMING BITS (IATR0<5:0>)

The Initial Analog Trimming Register allows +32ppm to -31ppm adjustment in 1ppm/bit increments. This enables fine frequency adjustment for trimming initial crystal accuracy error or to correct for aging drift.

The ISL12020M has a preset Initial Analog Trimming value corresponding to the crystal in the module. This value is recalled on initial power-up and should never be changed for best temperature compensation performance, although the user may change this preset value to adjust for aging or board mounting changes if so desired.

The IATR0 register should only be changed while the TSE (Temp Sense Enable) bit is “0”.

TABLE 11. INITIAL AT AND DT SETTING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Bh	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00

TABLE 12. IATRO TRIMMING RANGE

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	TRIMMING RANGE
0	**0**	**0**	**0**	**0**	**0**	**+32**
0	0	0	0	0	1	+31
0	0	0	0	1	0	+30
0	0	0	0	1	1	+29
0	0	0	1	0	0	+28
0	0	0	1	0	1	+27
0	0	0	1	1	0	+26
0	0	0	1	1	1	+25
0	0	1	0	0	0	+24
0	0	1	0	0	1	+23
0	0	1	0	1	0	+22
0	0	1	0	1	1	+21
0	0	1	1	0	0	+20
0	0	1	1	0	1	+19
0	0	1	1	1	0	+18
0	0	1	1	1	1	+17
0	1	0	0	0	0	+16
0	1	0	0	0	1	+15
0	1	0	0	1	0	+14
0	1	0	0	1	1	+13
0	1	0	1	0	0	+12
0	1	0	1	0	1	+11
0	1	0	1	1	0	+10
0	1	0	1	1	1	+9
0	1	1	0	0	0	+8
0	1	1	0	0	1	+7
0	1	1	0	1	0	+6
0	1	1	0	1	1	+5
0	1	1	1	0	0	+4
0	1	1	1	0	1	+3
0	1	1	1	1	0	+2

TABLE 12. IATRO TRIMMING RANGE (Continued)

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	TRIMMING RANGE
0	1	1	1	1	1	+1
1	0	0	0	0	0	0
1	0	0	0	0	1	-1
1	0	0	0	1	0	-2
1	0	0	0	1	1	-3
1	0	0	1	0	0	-4
1	0	0	1	0	1	-5
1	0	0	1	1	0	-6
1	0	0	1	1	1	-7
1	0	1	0	0	0	-8
1	0	1	0	0	1	-9
1	0	1	0	1	0	-10
1	0	1	0	1	1	-11
1	0	1	1	0	0	-12
1	0	1	1	0	1	-13
1	0	1	1	1	0	-14
1	0	1	1	1	1	-15
1	1	0	0	0	0	-16
1	1	0	0	0	1	-17
1	1	0	0	1	0	-18
1	1	0	0	1	1	-19
1	1	0	1	0	0	-20
1	1	0	1	0	1	-21
1	1	0	1	1	0	-22
1	1	0	1	1	1	-23
1	1	1	0	0	0	-24
1	1	1	0	0	1	-25
1	1	1	0	1	0	-26
1	1	1	0	1	1	-27
1	1	1	1	0	0	-28
1	1	1	1	0	1	-29
1	1	1	1	1	0	-30
1	1	1	1	1	1	-31

ALPHA Register (ALPHA)

TABLE 13. ALPHA REGISTER

ADDR	7	6	5	4	3	2	1	0
0Ch	ALPHA 7	ALPHA 6	ALPHA 5	ALPHA 4	ALPHA 3	ALPHA 2	ALPHA 1	ALPHA 0

The ALPHA variable is 8 bits and is defined as the temperature coefficient of crystal from -40°C to T0, or the ALPHA Cold (There is an Alpha Hot register that must be programmed as well). It is normally given in units of ppm/°C^2, with a typical value of -0.034. The ISL12020M device uses a scaled version of the absolute value of this coefficient in order to get an integer value. Therefore, ALPHA<7:0> is defined as the (|Actual ALPHA Value| x 2048) and converted to binary. For example, a crystal with Alpha of -0.034ppm/°C^2 is first scaled (|2048*(-0.034)| = 70d) and then converted to a binary number of 01000110b.

The practical range of Actual ALPHA values is from -0.020 to -0.060.

The ISL12020M has a preset ALPHA value corresponding to the crystal in the module. This value is recalled on initial power-up and should remain unchanged for best compensation performance, although the user can override this preset value if so desired.

The ALPHA register should only be changed while the TSE (Temp Sense Enable) bit is “0”. Note that both the ALPHA and the ALPHA Hot registers need to be programmed with values for full range temperature compensation.

BETA Register (BETA)

TABLE 14.

ADDR	7	6	5	4	3	2	1	0
0Dh	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0

TEMPERATURE SENSOR ENABLED BIT (TSE)

This bit enables the Temperature Sensing operation, including the temperature sensor, A/D converter and FATR/FDTR register adjustment. The default mode after power-up is disabled
(TSE = 0). To enable the operation, TSE should be set to 1 (TSE = 1). When temp sense is disabled, the initial values for IATR and IDTR registers are used for frequency control.

All changes to the IDTR, IATR, ALPHA and BETA registers must be made with TSE = 0. After loading the new values, TSE can be enabled and the new values are used. When TSE is set to 1, the temperature conversion cycle begins and will end when two temperature conversions are completed. The average of the two conversions is in the TEMP registers.

TEMP SENSOR CONVERSION IN BATTERY MODE BIT (BTSE)

This bit enables the Temperature Sensing and Correction in battery mode. BTSE = 0 default no conversion in battery mode. BTSE = 1 Temp Sensing enabled in battery mode. The BTSE is disabled when the battery voltage is lower than 2.6V.

FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT (BTSR)

This bit controls the frequency of Temp Sensing and Correction. BTSR = 0 default mode is every 10 minutes, BTSR = 1 is every 1.0 minute. Note that BTSE has to be enabled in both cases. See Table 15.

TABLE 15. FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT

BTSE	BTSR	TC PERIOD IN BATTERY MODE
0	0	OFF
0	1	OFF
1	0	10 Minutes
1	1	1 Minute

GAIN FACTOR OF AT BIT (BETA<4:0>)

Beta is specified to take care of the Cm variations of the crystal. Most crystals specify Cm around 2.2fF. For example, if Cm > 2.2fF, the actual AT steps may reduce from 1ppm/step to approximately 0.80ppm/step. Beta is then used to adjust for this variation and restore the step size to 1ppm/step.

BETA values are limited in the range from 01000 to 11111 as shown in Table 16**.** To use Table 16, the device is tested at two AT settings as follows:

BETA VALUES = (AT(max) - AT (min))/63, where:

AT(max) = F_{OUT} in ppm (at AT = 00H) and

AT(min) = F_{OUT} in ppm (at AT = 3FH).

The BETA VALUES result is indexed in the right hand column and the resulting Beta factor (for the register) is in the same row in the left column.

The ISL12020M has a preset BETA value corresponding to the crystal in the module. This value is recalled on initial power-up and should never be changed for best temperature compensation performance, although the user may override this preset value if so desired.

The value for BETA should only be changed while the TSE (Temp Sense Enable) bit is “0”. The procedure for writing the BETA register involves two steps. First, write the new value of BETA with TSE = 0. Then write the same value of BETA with TSE = 1. This will insure the next temp sense cycle will use the new BETA value**.**

TABLE 16. BETA VALUES

BETA<4:0>	AT STEP ADJUSTMENT
01000	0.5000
00111	0.5625
00110	0.6250
00101	0.6875
00100	0.7500
00011	0.8125
00010	0.8750
00001	0.9375
00000	1.0000
10000	1.0625

TABLE 16. BETA VALUES (Continued)

BETA<4:0>	AT STEP ADJUSTMENT
10001	1.1250
10010	1.1875
10011	1.2500
10100	1.3125
10101	1.3750
10110	1.4375
10111	1.5000
11000	1.5625
11001	1.6250
11010	1.6875
11011	1.7500
11100	1.8125
11101	1.8750
11110	1.9375
11111	2.0000

Final Analog Trimming Register (FATR)

This register shows the final setting of AT after temperature correction. It is read-only; the user cannot overwrite a value to this register. This value is accessible as a means of monitoring the temperature compensation function. See Table 17 and Table 12 (for values)/

TABLE 17. FINAL ANALOG TRIMMING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Eh	0	0	FATR5	FATR4	FATR3	FATR2	FATR1	FATR0

Final Digital Trimming Register (FDTR)

This Register shows the final setting of DT after temperature correction. It is read-only; the user cannot overwrite a value to this register. The value is accessible as a means of monitoring the temperature compensation function. The corresponding clock adjustment values are shown in Table 19. The FDTR setting has both positive and negative settings to adjust for any offset in the crystal.

TABLE 18. FINAL DIGITAL TRIMMING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Fh	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0

TABLE 19. CLOCK ADJUSTMENT VALUES FOR FINAL DIGITAL TRIMMING REGISTER

FDTR<2:0>	DECIMAL	ppm ADJUSTMENT
00000	0	0
00001	1	30.5
00010	2	61
00011	3	91.5

TABLE 19. CLOCK ADJUSTMENT VALUES FOR FINAL DIGITAL TRIMMING REGISTER (Continued)

FDTR<2:0>	DECIMAL	ppm ADJUSTMENT
00100	4	122
00101	5	152.5
00110	6	183
00111	7	213.5
01000	8	244
01001	9	274.5
01010	10	305
10000	0	0
10001	-1	-30.5
10010	-2	-61
10011	-3	-91.5
10100	-4	-122
10101	-5	-152.5
10110	-6	-183
10111	-7	-213.5
11000	-8	-244
11001	-9	-274.5
11010	-10	-305

ALARM Registers (10h to 15h)

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the bit 7 on any of the Alarm registers (ESCA0... EDWA0) to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the Alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}/F_{OUT}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting the bit 7 on any of the Alarm registers (ESCA0... EDWA0) to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}/F_{OUT}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or

daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear a single event alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to 1 (address 08h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1

- Alarm set with single interrupt (IM = ”0”)
- A single alarm will occur on January 1 at 11:30 a.m.
- Set Alarm registers as follows:

ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to “1” and also bringing the $\overline{IRQ}/F_{OUT}$ output low.

Example 2

- Pulsed interrupt once per minute (IM = ”1”)
- Interrupts at one minute intervals when the seconds register is at 30 seconds.
- Set Alarm registers as follows:

ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

Once the registers are set, the following waveform will be seen at $\overline{IRQ}/F_{OUT}$:

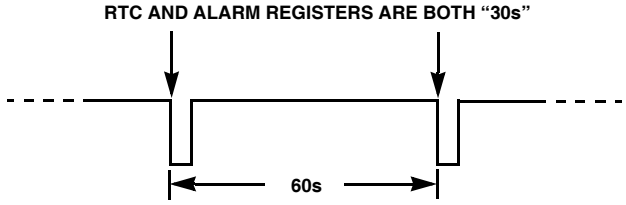


FIGURE 4. $\overline{IRQ}/F_{OUT}$ WAVEFORM

Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

Time Stamp V_{DD} to Battery Registers (TSV2B)

The TSV2B Register bytes are identical to the RTC register bytes, except they do not extend beyond the Month. The Time Stamp captures the FIRST V_{DD} to Battery Voltage transition time, and will not update upon subsequent events, until cleared (only the first event is captured before clearing). Set CLRTS = 1 to clear this register (Add 09h, PWR_V_{DD} register).

Note that the time stamp registers are cleared to all “0”, including the month and day, which is different from the RTC and alarm registers (those registers default to 01h). This is the indicator that no time stamping has occurred since the last clear or initial power-up. Once a time stamp occurs, there will be a non-zero time stamp.

Time Stamp Battery to V_{DD} Registers (TSB2V)

The Time Stamp Battery to V_{DD} Register bytes are identical to the RTC register bytes, except they do not extend beyond Month. The Time Stamp captures the LAST transition of V_{BAT} to V_{DD} (only the last event of a series of power up/down events is retained). Set CLRTS = 1 to clear this register (Add 09h, PWR_V_{DD} register).

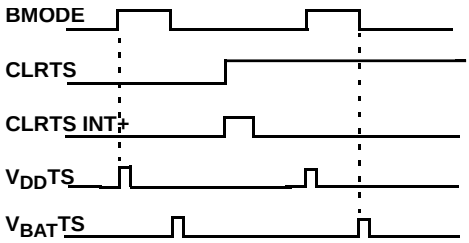


FIGURE 5.

TABLE 20. DST FORWARD REGISTERS

ADDRESS	FUNCTION	7	6	5	4	3	2	1	0
15h	**Month Forward**	DSTE	0	0	MoFd20	MoFd13	MoFd12	MoFd11	MoFd10
16h	**Day Forward**	0	DwFdE	WkFd12	WkFd11	WkFd10	DwFd12	DwFd11	DwFd10
17h	**Date Forward**	0	0	DtFd21	DtFd20	DtFd13	DtFd12	DtFd11	DtFd10
18h	**Hour Forward**		0	HrFd21	HrFd20	HrFd13	HrFd12	HrFd11	HrFd10

TABLE 21. DST REVERSE REGISTERS

ADDRESS	NAME	7	6	5	4	3	2	1	0
19h	**Month Reverse**	0	0	0	MoRv20	MoRv13	MoRv12	MoRv11	MoRv10
1Ah	**Day Reverse**	0	DwRvE	WkRv12	WkRv11	WkRv10	DwRv12	DwRv11	DwRv10
1Bh	**Date Reverse**	0	0	DtRv21	DtRv20	DtRv13	DtRv12	DtRv11	DtRv10
1Ch	**Hour Reverse**		0	HrRv21	HrRv20	HrRv13	HrRv12	HrRv11	HrRv10

DST Control Registers (DSTCR)

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning (set Forward) time is controlled by the registers DstMoFd, DstDwFd, DstDtFd, and DstHrFd. DST ending time (set Backward or Reverse) is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

Tables 20 and 21 describe the structure and functions of the DSTCR.

DST FORWARD REGISTERS (20H TO 23H)

DSTE is the DST Enabling Bit located in bit 7 of register 15h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time (including battery), the DSTE bit defaults to “0”.

DST forward is controlled by the following DST Registers:

DstMoFd sets the Month that DST starts. The default value for the DST begin month is April (04h)**.**

DstDwFd sets the Day of the Week that DST starts. DstDwFdE sets the priority of the Day of the Week over the Date. For DstDwFdE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Forward Day of the Week is Sunday (00h).

DstDtfd controls which Date DST begins. The default value for DST forward date is on the first date of the month (01h). DstDtFd is only effective if DstDwFdE = 0.

DstHrFd controls the hour that DST begins. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrFd registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value for DST hour is 2:00AM (02h). The time is advanced from 2:00:00AM to 3:00:00AM for this setting.

DST REVERSE REGISTERS (24H TO 27H)

DST end (reverse) is controlled by the following DST Registers.

DstMoRv sets the Month that DST ends. The default value for the DST end month is October (10h).

DstDwRv controls the Day of the Week that DST should end. The DwRvE bit sets the priority of the Day of the Week over the Date. For DwRvE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for DST DwRv end is Sunday (00h).

DstDtRv controls which Date DST ends. The default value for DST Date Reverse is on the first date of the month. The DstDtRv is only effective if the DwRvE = 0.

DstHrRv controls the hour that DST ends. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrRv registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value sets the DST end at 2:00AM. The time is set back from 2:00:00AM to 1:00:00AM for this setting.

TEMP Registers (TEMP)

The temperature sensor produces an analog voltage output which is input to an A/D converter and produces a 10-bit temperature value in degrees Kelvin. TK07:00 are the LSBs of the code, and TK09:08 are the MSBs of the code. The temperature result is actually the average of two successive temperature measurements to produce greater resolution for the temperature control. The output code can be converted to degrees Centigrade by first converting from binary to decimal, dividing by 2, and then subtracting 273d.

$$\text{Temperature in °C} = [(TK\langle 9{:}0\rangle)/2] - 273 \quad \text{(EQ. 1)}$$

The practical range for the temp sensor register output is from 446d to 726d, or -50°C to +90°C. The temperature compensation function is only guaranteed over -40°C to +85°C. The TSE bit must be set to “1” to enable temperature sensing.

TABLE 22.

TEMP	7	6	5	4	3	2	1	0
TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00
TK0M	0	0	0	0	0	0	TK09	TK08

NPPM Registers (NPPM)

The NPPM value is exactly 2 times the net correction required to bring the oscillator to 0ppm error. The value is the combination of oscillator Initial Correction (IPPM) and crystal temperature dependent correction (CPPM).

IPPM is used to compensate the oscillator offset at room temperature and is controlled by the ITR0 and BETA registers which are fixed during factor test.

The CPPM compensates the oscillator frequency fluctuation over temperature. It is determined by the temperature (T), crystal curvature parameter (ALPHA), and crystal turnover temperature (XT0). T is the result of the temp sensor/ADC conversion, whose decimal result is 2 times the actual temperature in Kelvin. ALPHA is from either the ALPHA (cold) or ALPHAH (hot) register depending on T, and XT0 is from the XT0 register.

NPPM is governed by the following equations:

NPPM=IPPM(ITR0,BETA) + ALPHA x (T-T0)2

$$NPPM = IPPM + CPPM$$

$$NPPM = IPPM + \frac{ALPHA \bullet (T - T0)^2}{4096} \quad \text{(EQ. 2)}$$

where

$$ALPHA = \alpha \bullet 2048$$

T is the reading of the ADC, result is 2 x temperature in degrees Kelvin.

$$T = (2 \bullet 298) + XT0 \quad \text{(EQ. 3)}$$

or $T = 596 + XT0$

Note that NPPM can also be predicted from the FATR and FDTR register by the relationship (all values in decimal):

NPPM=2*(BETA*FATR - (FDTR-16))

XT0 Registers (XT0)

TURNOVER TEMPERATURE (XT<3:0>)

The apex of the Alpha curve occurs at a point called the turnover temperature, or XT0. Crystals normally have a turnover temperature between +20°C and +30°C, with most occurring near +25°C.

TABLE 23. TURNOVER TEMPERATURE

ADDR	7	6	5	4	3	2	1	0
2Ch	0	0	0	XT4	XT3	XT2	XT1	XT0

The ISL12020M has a preset Turnover temperature corresponding to the crystal in the module. This value is recalled on initial power-up and should never be changed for best temperature compensation performance, although the user may override this preset value if so desired.

Table 23 shows the values available, with a range from +17.5°C to +32.5°C in +0.5°C increments. The default value is 00000b or +25°C.

TABLE 24. XT0 VALUES

XT<4:0>	TURNOVER TEMPERATURE
01111	32.5
01110	32.0
01101	31.5
01100	31
01011	30.5
01010	30
01001	29.5
01000	29.0
00111	28.5
00110	28.0
00101	27.5
00100	27.0
00011	26.5
00010	26.0
00001	25.5
00000	25.0
10000	25.0
10001	24.5
10010	24.0
10011	23.5
10100	23.0
10101	22.5
10110	22.0
10111	21.5
11000	21.0
11001	20.5
11010	20.0
11011	19.5
11100	19.0
11101	18.5
11110	18.0
11111	17.5

ALPHA Hot Register (ALPHAH)

TABLE 25. ALPHA REGISTER

ADDR	7	6	5	4	3	2	1	0
2Dh	ALP_H7	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0

The ALPHA Hot variable is 7 bits and is defined as the temperature coefficient of Crystal from the XT0 value to +85°C (both Alpha Hot and Alpha Cold must be programmed to provide full temperature compensation). It is normally given in units of ppm/°C^2, with a typical value of -0.034. Like the ALPHA Cold version, a scaled version of the absolute value of this coefficient is used in order to get an integer value. Therefore, ALP_H<7:0> is defined as the (|Actual Alpha Hot Value| x 2048) and converted to binary. For example, a crystal with Alpha Hot of -0.034ppm/°C^2 is first scaled (|2048*(-0.034)| = 70d) and then converted to a binary number of 01000110b.

The practical range of Actual ALPHAH values is from -0.020 to -0.060.

The ISL12020M has a preset ALPHAH value corresponding to the crystal in the module. This value is recalled on initial power-up and should never be changed for best temperature compensation performance, although the user may override this preset value if so desired.

The ALPHAH register should only be changed while the TSE (Temp Sense Enable) bit is “0”.

User Registers (Accessed by Using Slave Address 1010111x)

Addresses [00h to 7Fh]

These registers are 128 bytes of battery-backed user SRAM. The separate I^{2}C slave address must be used to read and write to these registers.

I^{2}C Serial Interface

The ISL12020M supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12020M operates as a slave device in all applications.

All communication over the I^{2}C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 6). On power-up of the ISL12020M, the SDA pin is in the input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12020M continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 6). A START condition is ignored during the power-up sequence.

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 6). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 7).

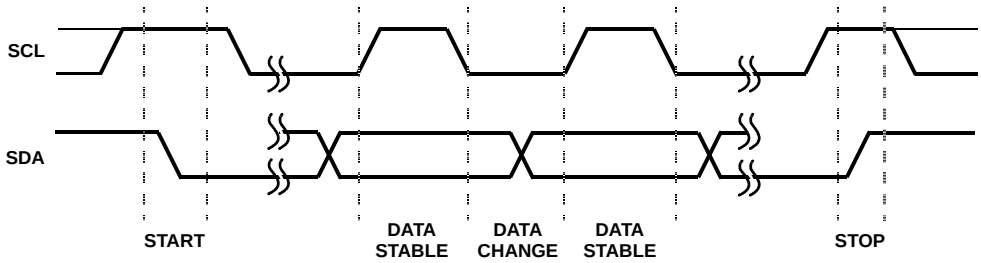


FIGURE 6. VALID DATA CHANGES, START AND STOP CONDITIONS

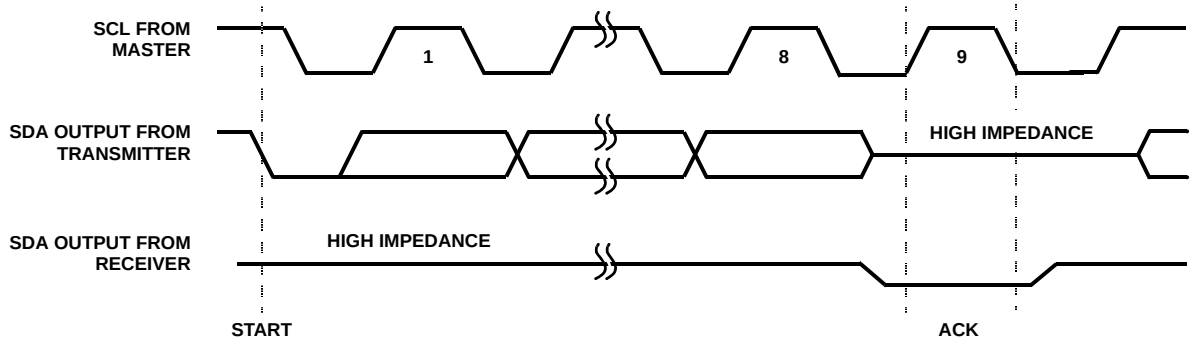


FIGURE 7. ACKNOWLEDGE RESPONSE FROM RECEIVER

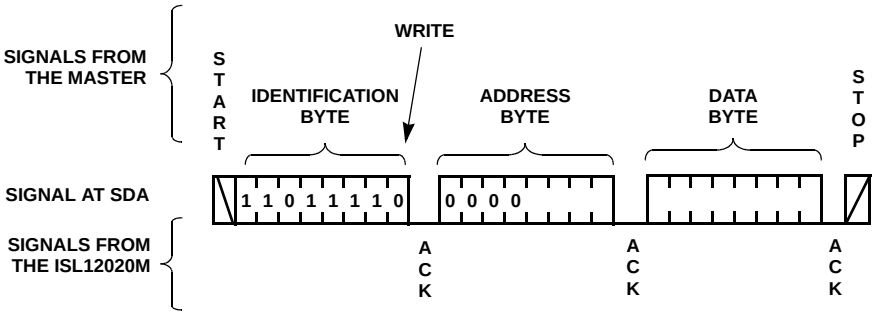


FIGURE 8. BYTE WRITE SEQUENCE (SLAVE ADDRESS FOR CSR SHOWN)

The ISL12020M responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL12020M also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifiers. These bits are “1101111” for the RTC registers and “1010111” for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, a read operation is selected. A “0” selects a write operation (refer to Figure 9).

After loading the entire Slave Address Byte from the SDA bus, the ISL12020M compares the device identifier and device select bits with “1101111” or “1010111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Bytes, as shown in Figure 10.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Control/Status Registers, the slave byte must be “1101111x” in both places.

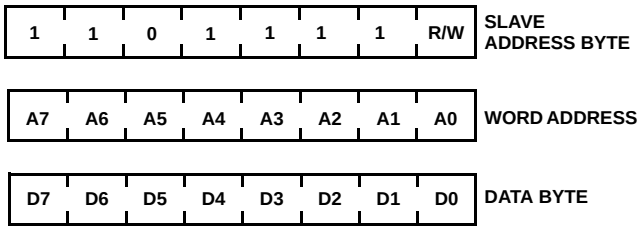


FIGURE 9. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12020M responds with an ACK. At this time, the I^2C interface enters a standby state.

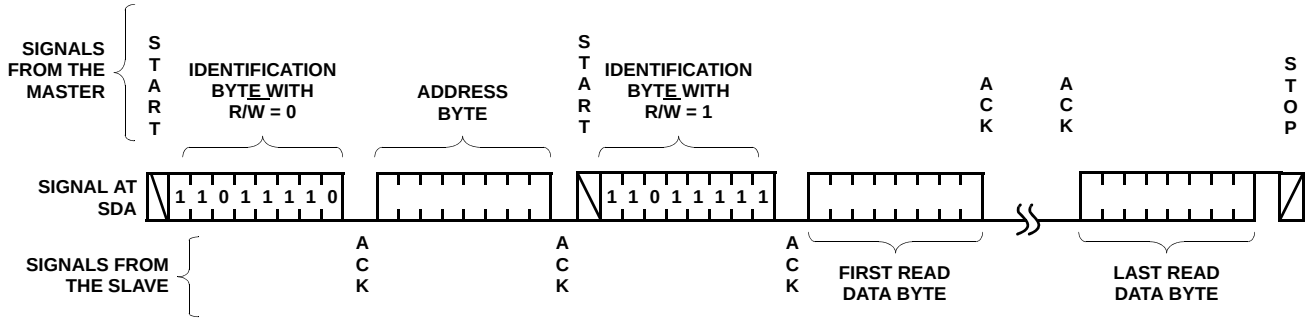


FIGURE 10. READ SEQUENCE (CSR SLAVE ADDRESS SHOWN)

Read Operation

A Read operation consists of a three byte instruction, followed by one or more Data Bytes (see Figure 10). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12020M responds with an ACK. Then the ISL12020M transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 10).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer’s initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13h, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

Application Section

Battery Backup Details

Many types of batteries can be used with the Intersil RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power an Intersil RTC device for up to 10 years. Another option is to use a supercapacitor for applications where V_{DD} may disappear intermittently for short periods of time. Depending on the value of supercapacitor used, backup time can last from a few days to two weeks (with >1F). A simple silicon or Schottky barrier diode can be used in series with V_{DD} to charge the supercapacitor, which is connected to the V_{BAT} pin. Try to use Schottky diodes with very low leakages, <10nA is desirable. Do not use the diode connection to charge a battery (especially lithium batteries!).

Layout Considerations

The crystal pins X1 and X2 have a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 11 shows a suggested layout for the ISL12020M device. Three main precautions should be followed:

- Do not run the serial bus lines or any high speed logic lines in the vicinity of the X1 and X2 pins. These logic level lines can induce noise in the oscillator circuit, causing misclocking.
- Add a ground trace around the device with one end terminated at the chip ground. This guard ring will provide termination for emitted noise in the vicinity of the RTC device.

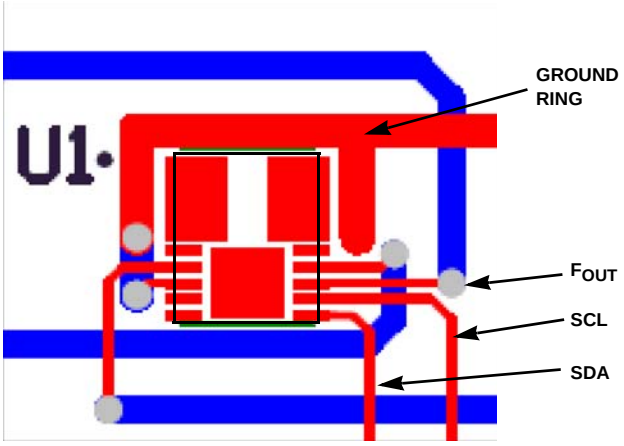


FIGURE 11. SUGGESTED LAYOUT FOR ISL12020M

- Do not run a ground or power plane immediately under the RTC. This will add capacitance to the X1/X2 pins and change the trimmed frequency of the oscillator. Instead, try to leave a gap in any planes under the RTC device.

The best way to run clock lines around the RTC is to stay outside of the ground ring by at least a few millimeters. Also, use the V_{BAT} and V_{DD} as guard ring lines as well, they can isolate clock lines from the X1 and X2 pins. In addition, if the $\overline{IRQ}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well.

Measuring Oscillator Accuracy

The best way to analyze the ISL12020M frequency accuracy is to set the $\overline{IRQ}/F_{OUT}$ pin for a specific frequency, and look at the output of that pin on a high accuracy frequency counter (at least 7 digits accuracy). Note that the $\overline{IRQ}/F_{OUT}$ is an drain output and will require a pullup resistor.

Using the 1.0Hz output frequency is the most convenient as the ppm error is just

ppm error = (F_{OUT} -1) x 1e6

Other frequencies may be used for measurement but the error calculation becomes more complex.

When the proper layout guidelines above are observed, the oscillator should start up in most circuits in less than one second. When testing RTC circuits, a common impulse is to apply a scope probe to the circuit at the X2 pin (oscillator output) and observe the waveform. DO NOT DO THIS! Although in some cases you may see a usable waveform, due to the parasitics (usually 10pF to ground) applied with the scope probe, there will be no useful information in that waveform other than the fact that the circuit is oscillating. The X2 output is sensitive to capacitive impedance so the voltage levels and the frequency will be affected by the parasitic elements in the scope probe. Use the F_{OUT} output and a frequency counter for the most accurate results.

Temperature Compensation Operation

The ISL12020M temperature compensation feature needs to be enabled by the user. This must be done in a specific order as follows.

1. Read register 0Dh, the BETA register. This register contains the 5-bit BETA trimmed value which is automatically loaded on initial power-up. Mask off the 5LSB's of the value just read.
2. Bit 7 of the BETA register is the master enable control for temperature sense operation. Set this to "1" to allow continuous temperature frequency correction. Frequency correction will then happen every 60seconds with V_{DD} applied.
3. Bits 5 and 6 of the BETA register control temperature compensation in battery backup mode (see Table 15). Set the values for the operation desired.
4. Write back to register 0Dh making sure not to change the 5 LSB values, and include the desired compensation control bits.

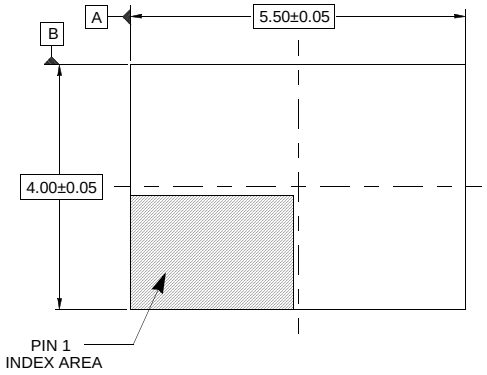
Note that every time the BETA register is written with the TSE bit = 1, a temperature compensation cycle is instigated and a new correction value will be loaded into the FATR/FDTR registers (if the temperature changed since the last conversion).

Also note that registers 0Bh and 0Ch, the ITR0 and ALPHA registers, should not be changed. If they must be written be sure to write the same values that are recalled from initial power-up. The ITR0 register may be written if the user wishes to re-calibrate the oscillator frequency at room temperature for aging or board mounting. The original recalled value can be re-written if desired after testing.

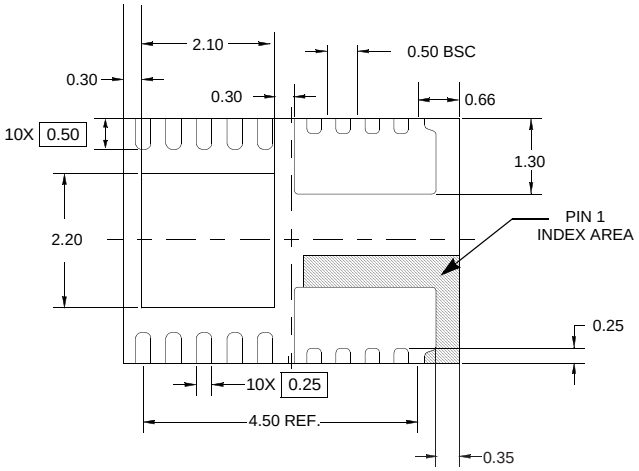
Package Outline Drawing

L20.4.0x5.5

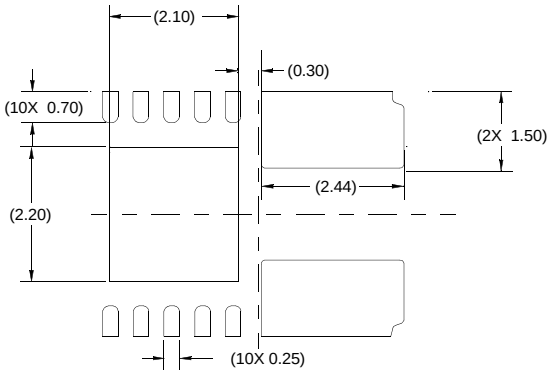
20 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 12/07



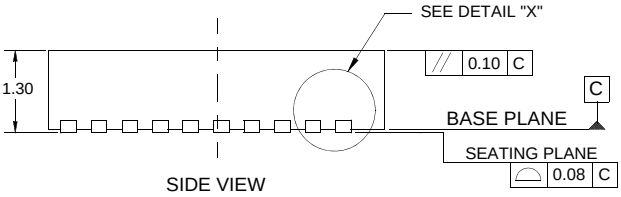
TOP VIEW



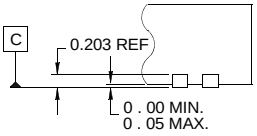
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
5. No other electrical connection allowed under backside of X1 or X2 areas.
6. The X1 and X2 pads need to be soldered down to the PCB on separate and electrically isolated land pads.